# Arithmetic operators for pairing-based cryptography 

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## Outline of the talk

- Pairings?
- Arithmetic over $\mathbb{F}_{3 m}$
- Unified operator
- Results
- Final thoughts


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- But there's more: bilinear pairings


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\hat{e}: G_{1} \times G_{1} \rightarrow G_{2}
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that satisfies the following conditions:

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- non-degeneracy: $\hat{e}(P, P) \neq 1_{G_{2}}$
- bilinearity: for all $Q_{1}, Q_{2}$ and $R \in G_{1}$,

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\hat{e}\left(Q_{1}+Q_{2}, R\right)=\hat{e}\left(Q_{1}, R\right) \hat{e}\left(Q_{2}, R\right) \quad \text { and } \quad \hat{e}\left(R, Q_{1}+Q_{2}\right)=\hat{e}\left(R, Q_{1}\right) \hat{e}\left(R, Q_{2}\right)
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- Immediate property: for any integer $a$,

$$
\hat{e}(a P, P)=\hat{e}(P, a P)=\hat{e}(P, P)^{a}
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- Menezes-Okamoto-Vanstone (MOV) attack, 1993
- One-round three-party key agreement (Joux, 2000)
- Identity-based encryption
- Boneh-Franklin, 2001
- Sakai-Kasahara, 2001
- ...
- Short signatures
- Boneh-Lynn-Shacham (BLS), 2001
- Zang-Safavi-Naini-Susilo (ZSS), 2004
- ...


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- Tate pairing
- $\eta_{T}$ pairing
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\hat{\eta_{T}}: E\left(\mathbb{F}_{3^{m}}\right)[\ell] \times E\left(\mathbb{F}_{3^{m}}\right)[\ell] \rightarrow \mu_{\ell} \subset \mathbb{F}_{3^{6 m}}
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| Operation | Count | $m=97$ |
| :---: | :---: | :---: |
| $+/-$ | $121\left\lfloor\frac{m}{4}\right\rfloor+186$ | 3090 |
| $\times$ | $25\left\lfloor\frac{m}{4}\right\rfloor+79$ | 679 |
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- Arithmetic over $\mathbb{F}_{3}$ :
- Polynomial basis: $\mathbb{F}_{3^{m}} \cong \mathbb{F}_{3}[x] /(f(x))$
- Degree- $m$ irreducible polynomial $f(x)$ carefully chosen


## Addition over $\mathbb{F}_{\mathbf{3}^{m}}$



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- coefficient-wise addition over $\mathbb{F}_{3}$


## Addition over $\mathbb{F}_{3}{ }^{m}$



- coefficient-wise addition over $\mathbb{F}_{3}$
- addition over $\mathbb{F}_{3}$ : small look-up table


## Addition, subtraction and accumulation over $\mathbb{F}_{3^{m}}$



- sign selection: multiplication by 1 or 2

$$
-a(x) \equiv 2 a(x) \quad(\bmod 3)
$$

- feedback loop for accumulation


## Multiplication over $\mathbb{F}_{3 \mathrm{~m}}$

- Parallel-serial multiplication
- multiplicand loaded in a parallel register
- multiplier loaded in a shift register
- Most significant coefficients first
- $D$ coefficients processed at each iteration: $\left\lceil\frac{m}{D}\right\rceil$ iterations per multiplication


## Multiplication over $\mathbb{F}_{3}{ }^{m}$



- partial product generator (PPG): $m$ multiplications over $\mathbb{F}_{3}$
- multiplication by $x^{i}$ : only wiring
- simple modular reductions


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- Example: $m=97$ and $f(x)=x^{97}+x^{12}+2$

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\begin{aligned}
a(x)^{3} \bmod f(x) & =\left(a_{32} x^{96}+a_{64} x^{95}+a_{96} x^{94}+\cdots+a_{33} x^{2}+a_{65} x+a_{0}\right) \times 1 \\
& +\left(0+a_{60} x^{95}+a_{88} x^{94}+\cdots+0+a_{61} x+a_{89}\right) \times 1 \\
& +\left(0+a_{60} x^{95}+a_{92} x^{94}+\cdots+0+a_{61} x+a_{93}\right) \times 1
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& +\left(0+a_{60} x^{95}+a_{92} x^{94}+\cdots+0+a_{61} x+a_{93}\right) \times 1 \\
& =w_{1} \cdot \nu_{1}(x)+w_{2} \cdot \nu_{2}(x)+w_{3} \cdot \nu_{3}(x)
\end{aligned}
$$

- Required hardware:
- only wires to compute the $\nu_{i}(x)$ 's
- possibly multiplications over $\mathbb{F}_{3}$
- multi-operand addition over $\mathbb{F}_{3 m}$


## Cubing over $\mathbb{F}_{\mathbf{3}^{m}}$



- feedback loop for successive cubings
- sign selection for computing either $a(x)^{3}$ or $-a(x)^{3}$


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- Extended Euclidean algorithm?


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- only one inversion for the full pairing: delay overhead is negligible ( $<1 \%$ )


## The full processing element



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- For the $\eta_{T}$ pairing:
almost no parallelism between additions, multiplications and cubings
- Can we share hardware resources between the three operators?


## Unified operator



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## Results

- Full co-processor for computation of the $\eta_{T}$ pairing
- field: $\mathbb{F}_{397}$ with $f(x)=x^{97}+x^{12}+2$
- processing element: unified operator with $D=3$
- prototype on a Xilinx Virtex-II Pro 4 FPGA


## Results

- Full co-processor for computation of the $\eta_{T}$ pairing
- field: $\mathbb{F}_{397}$ with $f(x)=x^{97}+x^{12}+2$
- processing element: unified operator with $D=3$
- prototype on a Xilinx Virtex-II Pro 4 FPGA
- Area: 1833 slices ( $63 \%$ of the FPGA) and 6 memory blocks (21\%)
- Clock frequency: 145 MHz
- Full $\eta_{T}$ pairing: 27800 clock cycles
- Computation time: $192 \mu \mathrm{~s}$


## Comparisons

| Architecture | Area | Time | FPGA |
| :---: | :---: | :---: | :---: |
| Proposed solution <br> (CHES'07) | 1833 slices | $192 \mu \mathrm{~s}$ | Virtex-II Pro |
| Grabher and Page <br> (CHES'05) | 4481 slices | $432 \mu \mathrm{~s}$ | Virtex-II Pro |
| Kerins et al. <br> (CHES'05) | 55616 slices | $850 \mu \mathrm{~s}$ | Virtex-II Pro |
| Ronan et al. <br> (ITNG'07) | 10000 slices | $178 \mu \mathrm{~s}$ | Virtex-II Pro |
| Beuchat et al. <br> (Arith'07 \& WAIFI'07) | 18000 LEs <br> Jiang <br> (Univ. Honk Kong, 2007) <br> 74000 slices) | $33 \mu \mathrm{~s}$ | Cyclone II |

## Conclusion

- Unified operator generator
- Arithmetic over $\mathbb{F}_{p^{m}} \cong \mathbb{F}_{p}[x] /(f(x))$ for given $p, m$ and $f(x)$
- Support for the following operations:
- addition
- multiplication
- Frobenius map $\left(a(x)^{p} \bmod f(x)\right)$
- inverse Frobenius map $(\sqrt[p]{a(x)} \bmod f(x))$


## Future work

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- simpler arithmetic
- better suited to FPGAs (fast multiplication)


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- Ate pairing
- Side-channel


## Thank you for your attention

## Questions?

